REMARKS/ARGUMENTS

Claims 1-20 are pending in the application. Reconsideration in view the following remarks is respectfully requested.

Claims 6-10 and 16-20 are rejected under the second paragraph of 35 U.S.C. 112, as being unclear to the Examiner how or where testing is performed. Claims 1-8 and 11-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Motika et al. (US Patent No. 5,983,380; 9 Nov. 1999 (issue date)). Claims 6-8, 9-10, 16-18, and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Rajski et al. (US Patent No. 6,557,129;filed: 23 Nov. 1999). Claims 9-10 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al. in view of Rajski et al. Claims 6-8 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior art in view of Swoboda et al. (US Patent No. 6,349,392; Filed: 14, July 1999). By this Amendment, claims 1, 3, 4, 6, 9, 11, 13, 14, 16, and 19 are amended for clarification purposes. Also, claims 6, 9, 16 and 19 are amended to overcome the 35 U.S.C. 112 second paragraph rejection. Claims 2 and 12 are cancelled without prejudice or disclaimer.

Applicant's respectfully submit nowhere do the cited references describe, suggest or teach "[a]n on-chip testing apparatus comprising: a test pattern generator to generate test data for a plurality of testing channels; and a weight selector coupled to said test pattern generator, said weight selector to store weighting values to bias data for at least one of said testing channels wherein said weight selector includes a weight storage register to store said weighting values and said weight selector is to selectively bias individual bits of said test data" (as in amended claim 1).

The Office Action asserts that Motika et al. ("Motika") depicts e.g., in Fig. 6 and related description in col. 1 line 25 et seq., the claimed on-chip testing apparatus comprising: a test pattern generator (Fig. 6 Numeral 12, col. 2 line 35) to generate test data for a plurality of testing channels; and a weight selector (Fig. 6 Numerals 118-126 with Numerals 138 and 142, Fig. 5, col. 2 line 35) coupled to said test pattern generator, said weight selector to store weighting values to bias data (e.g., col. 2 line 62) for at least one of said testing channels.

Line 35 of column 2 of Motika discloses a BIST (Built In Self Test) design and a WRP (Weighted Random Pattern) test methodology. Column 2 line 62 of Motika states:

> "These patterns are then biased or weighted to optimize them for a specific logic design. In addition, a Multiple Input Signature Register (MISR) is used to compress the DUT responses into a signature for eventual comparison to a predetermined good signature".

Applicant respectfully submits that nowhere in Motika (including the Figures and cited sections) is the disclosure, teaching or suggestion of at least the limitation "...wherein said weight selector includes a weight storage register to store said weighting values and said weight selector is to *selectively bias individual bits of said test data*" as claimed in the embodiment of amended claim 1. Further support can be found in the specification at page 5 line 13, which states:

> "The weight storage register can also be useful in forcing a segment of an LBIST scan channel to a deterministic value every time a scan load takes place. In other words, each bit of the segment can be set to a desired value".

Therefore, since each and every limitation of the claimed embodiment is not covered by cited references, the 102(b) rejection is lacking and should be withdrawn. Amended independent claims 4, 6, 11, 14 and 16 contain substantively similar limitations, and therefore the 102(b) rejection for these claims should be withdrawn as

well. Claims 3, 5, 7-8, 13, 15, and 17-18 depend from the independent claims discussed above and therefore should be allowed as well.

Second, Applicant additionally submits that Rajski et al. ("Rajski") does not teach, suggest or disclose "[a]n on-chip testing apparatus comprising: channel filtering logic to receive data from a plurality of testing channels, said channel filtering logic to mask output data from a selected testing channel wherein in biasing test data, said biasing is performed selectively on individual bits of said test data" (as in amended claim 9).

The Office Action states that Rajski's Fig. 6 anticipates such claims because scan chains 44 are effectively blocked or masked via control block 46 prior to compaction by block 48 (also refer to Fig. 10 for logic implementation and also to col. 3 line 12, col. 13 lines 41-49 and col. 7 line 41 et seq., and MISR in Fig. 2: Block 22). Column 3 line 12 states:

> "[a]n ideal compaction algorithm has the following features: (1) it is easy to implement as a part of the on-chip test circuitry, (2) it is not a limiting factor with respect to test time, (3) it provides a logarithmic compression of the test data, and (4) it does not lose information concerning faults".

Column 13 lines 41-49 state:

> "[a] method for selectively compacting test responses of an integrated circuit, comprising: passing N test responses in an integrated circuit to a selector circuit; using the selector circuit, selectively preventing between 0 and N of the test responses from being passed to a compactor while allowing the remaining test responses to be passed to the compactor; and compacting the test responses passed to the compactor by the selector circuit; controlling the selector circuit via an external ATE".

Column 7 line 41 states:

> "[a]lthough FIG. 10 shows only a single control line, additional control lines can be used to mask different groups of scan chains".

However, nowhere in Rajski (including the Figures and cited sections discussed immediately above) is the disclosure, teaching or suggestion of at least the limitation

"...wherein in biasing test data, *said biasing is performed selectively on individual bits of said test data*" as claimed in the embodiment of amended claim 9. Since each and every limitation of the claimed embodiment is not covered by cited references, the 102(e) rejection is lacking and should be withdrawn. Amended independent claims 6, 16 and 19 contain substantively similar limitations, and therefore the 102(e) rejection for these claims should be withdrawn as well. Claims 7-8, 10, 17-18, and 20 depend from independent claims 6, 9, 16 and 19, and therefore should be allowed as well.

Third, the Office Action rejects claims 9-10 and 19-20 under 35 U.S.C. 103 (a) as being unpatentable over Motika in view of Rajski. The Office Action states:

> As per Claims 9, 19, Motika et al. substantially depicts, in Fig. 6 and related description in col. 2 line 25, the claimed on-chip testing apparatus comprising: channel filtering logic to receive data from a plurality of testing channels, said channel filtering logic to select or mask output data from a selected testing channel, e.g., in Fig. 6: MUX receives inputs from left-most BS chain and right-most SRL chain to effect selection control to MISR. Not specifically described in detail in Motika et al. is the step of output data masking. However Rajski et al., in an analogous art, discloses a testing methodology wherein such techniques are described.

Column 2 line 25 states:

> "[w]hile the prior art testing methods were suitable for testing devices of the then-existing complexity, the increase in circuit density requires more sophisticated testing techniques, not only to reduce testing time, but to assure the functional integrity of these devices".

Column 4 lines 43-47 state:

> "[g]enerally, the present invention combines a flat random BIST structure and a modified WRP concept into an extended BIST design. This design integrates on-chip the weighted pattern generation with external weight selection".

However, Applicant again respectfully submits that neither Rajski nor Motika teach, suggest or disclose anywhere "[a]n on-chip testing apparatus comprising: channel filtering logic to receive data from a plurality of testing channels, said channel filtering

logic to mask output data from a selected testing channel wherein in biasing test data, *said biasing is performed selectively on individual bits of said test data*" (as in amended claim 9). Therefore since neither Rajski nor Motika reference teach, suggest or disclose at least the claimed limitation "...wherein in biasing test data, said biasing is performed selectively on individual bits of said test data", the combination of both does not either. Since each and every limitation is not covered by the cited prior art, the 103 (a) rejection is lacking and should be withdrawn. Amended independent claim 19 contains substantively similar limitations and is allowable for similar reasons. Claims 10 and 20 depend from allowable independent claims and therefore should be allowed as well.

Lastly, the Office Action rejects claims 6-8 and 16-18 under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior art in view of Swoboda et al. ("Swoboda"). It states:

> As per Claims 6-8, 16-18, Admitted prior art substantially discloses the claimed the claimed on-chip testing means comprising: ... Not specifically described in detail in Admitted prior art is the step of clock stopping means along with associated hardware for implementation thereof. However Swoboda et al., in an analogous art, discloses a testing methodology in "*Devices, systems and methods for mode driven stops,* "wherein such techniques are described.

Column 14 lines 14-27 state:

> The analysis circuitry includes condition sensors such as hardware breakpoint sensors for controlled stops and tract stack circuitry for real-time trace recordkeeping. The analysis circuitry is serial-scan accessible and designated the analysis domain 1217. All peripherals including memory and serial and parallel ports are denominated as the system domain 1215. For uniformity of description, JTAG control 1201 is regarded as a clock domain also in which test clock JCLK is active. Emulation control circuitry 1203 is a further domain of FIG. 32. Special message passing circuitry 1216 is also included in the system or analysis domain, to even more fully use the host computer 1101 as an attached processor by interfacing the TIBUS to the serial scan line 1103 of FIG. 45. FIG. 53 shows a physical perspective of the various domains on the chip of device 11.

Column 20 line 9 states:

> Data and control information are scanned into and out of the domains on test clock JCLK, and the domains are independently and selectively started on functional clock FCLK and stopped, in extensive sequences to accomplish emulation, simulation and test functions with a wide degree of flexibility as circumstances of the development, manufacturing and field environments dictate.

However, Applicant again respectfully submits that neither Applicant's Admitted prior art nor Swoboda teach, suggest or disclose "[a] method of performing on-chip testing comprising: selectively supplying functional clocking signals to a plurality of testing channels to operate logic in said testing channels wherein in biasing test data, said biasing is performed selectively on individual bits of said test data" (as in amended claim 16). Therefore since neither the Applicant's Admitted prior art nor Swoboda teach, suggest or disclose at least the claimed limitation "*...wherein in biasing test data, said biasing is performed selectively on individual bits of said test data*", the combination of both does not either. Since each and every limitation is not covered by the cited prior art, the 103 (a) rejection is lacking and should be withdrawn. Amended independent claim 6 contains substantively similar limitations and is allowable for similar reasons. Claims 7-8 and 17-18 depend from allowable independent claims and therefore should be allowed as well.

For at least all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

Dated: July 7, 2004 By: _____

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